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[54] **OPTICAL READER KIT FOR LETTER SORTING MACHINES**

[75] Inventors: **Sebastian J. Lazzarotti**, Broomall; **Paul E. Tartar**, Chester, both of Pa.

[73] Assignee: **Burroughs Corporation**, Detroit, Mich.

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[51] **Int. Cl.**³ **G06K 7/00**; G06K 19/08

[52] **U.S. Cl.** **235/462**; 209/584

[58] **Field of Search** ..... 235/462, 375; 340/146.3 H; 209/3.2, 584, 610, 629, 569

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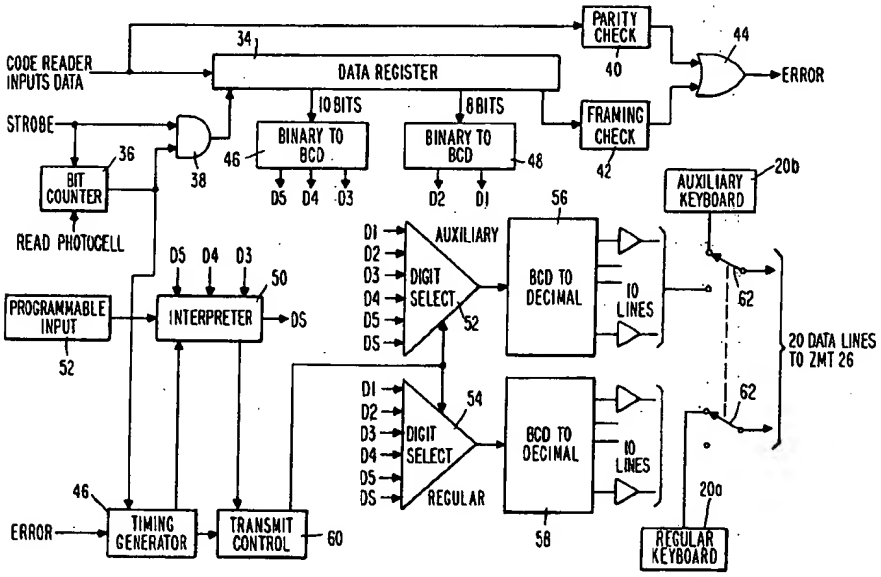
Primary Examiner—Donald J. Yusko

Attorney, Agent, or Firm—Francis A. Varallo; David G. Rasmussen; Kevin R. Peterson

[57] **ABSTRACT**

An optical reader system configured as a kit for retrofitting the input consoles of existing letter sorting machines of the type used by the U.S. Postal Service. Such machines require that an operator, stationed at a console, enter sorting information for each mail piece, by way of a manually actuated keyboard. The present invention expands the processing capabilities of the machines by permitting the machine reading of mail pieces that have had their address information precoded in machine readable form on their respective faces. At the same time, the automatic function does not impair or modify the usual operator controlled console operation when non-coded mail is being processed.

10 Claims, 4 Drawing Figures



54, which are designated respectively as being auxiliary and regular. The data outputs from the selectors 52 and 54 in BCD form are applied respectively to a pair of BCD-to-decimal converters 56 and 58, each of which includes 10 output lines for transmitting the mail destination data to the ZMT 26. The transmission of the data is controlled by the timing generator 46, the transmit control unit 60, and the logic within interpreter 50. Switching means 62 which may be mechanical or electronic are provided for switching from the "auto read" to the "manual keyboard" mode. In either case, twenty data lines output the desired information to the ZMT 26.

FIG. 4 provides more detailed information on the interpreter 50, transmit control 60 and timing generator 46 shown in FIG. 3. As mentioned in connection with the latter Figure, the purpose of the interpreter logic is to examine the first three digits of the ZIP code as read by the optical reader 10. In this examination, the interpreter 50 will determine whether the three digits match any of the auxiliary key assignments and if so, which key matches. The interpreter then supplies the proper information to the transmit control 60 which submits the code to the ZMT 26 in the proper format.

With general reference to FIG. 3, and specific reference to FIG. 4, the interpreter 50 is programmed by a programmable input unit 52 comprised of a set of BCD switches 64. For example, the latter may be of the thumbwheel type or dual-in-line printed circuit mounted digital switches. In either case, a switch 64 is required for each decimal digit. Thirty switches would be needed for a ten key capability, arranged in groups of three. The output switch signals from the programmable input unit 52 are applied to a multiplexer 66 which is addressed by a decode counter 68, which receives a clear signal input from the read photocell. The output of the multiplexer 66 is one of a group of three digits. The latter are applied to a comparator 70, which compares them to the digits D5, D4 and D3 read by the code reader 10. The decode counter 68 addresses each set of switches 64 and is stepped by clock and $\phi 1$ enable pulses supplied from the timing generator 46. If a match is found by the comparator 70, it applies to stop pulse to the counter 68. The BCD switches 64 are connected to the multiplexer 66 in such a way that the address into the multiplexer at the time of a match, represents the decimal number of the auxiliary keyboard 20*b* key assigned to the code producing the match. Therefore the address becomes the special digit, DS.

The counter 68 is controlled by signals from the timing generator 46. The timing generator 46 is comprised of an oscillator 72, for example of 1 KHz frequency, a divide-by-ten counter 74, which then produces a 100 Hz signal, and a sequence signal shift register 76. In this way two unconditional clocks are generated at respective frequencies of 1 KHz and 100 Hz. When the reader bit counter 36 (FIG. 3) reaches a count of twenty and no parity or framing error exists, the sequence shift register 76 is loaded and a series of sequenced signals $\phi 1$ through $\phi 6$ are generated thereby. During sequence $\phi 1$, the interpreter multiplexer counter 68 counts, and scans the switch inputs for a match. Sequence signals $\phi 2$ through $\phi 6$ are used by the logic circuits of the transmit control 60.

The transmit control 60 is made up of an encoder 78, a counter 80, and a format control programmable read-only memory (PROM) 82. A ROM may be substituted for the latter in certain applications. The encoder 78 receives signals from the keying mode switch 84, and the interpreter comparator 70. In effect, the encoder 78 is comprised of combinational logic and provides a 16 line to 4 line encode function. The combinational logic examines the comparator output and the keying switch mode, that is "2 digit" or "three digit and special", and selects one of 16 lines into the final encoder. For example, if A=B in the comparator 70 and the keying switch 84 is in the three digit mode, line 1 could be selected. This would result in a BCD code being loaded into the transmit control counter 80 by the $\phi 2$ pulse. The BCD code specifies the starting address of the count, and since the output of the counter 80 addresses the PROM 82, it selects the start point for the format required. Other combinations like $A \neq B$ and a three digit mode result in a different start point for the PROM, and therefore, a different transmit format. The counter 60 is stepped through three addresses by signals $\phi 3$, $\phi 4$ and $\phi 5$ applied thereto. The output of PROM 82 addresses the digit select units 52 and 54, each of which functions as a multiplexer, and select a BCD digit for transmission over regular or auxiliary key lines. The $\phi 6$ signal from the shift sequencer 76 clears the counter 80 and terminates the transmit sequence.

In conclusion, there has been described a code reader kit which has particular application in the retrofit of existing letter sorting machines. The ability of such machines to selectively operate in a manual mode, as at present, or in an automatic mode, as provided by the present invention, greatly increases the performance and usefulness of such machines. While there have been disclosed specific design details applicable to a particular machine, the basic principles taught herein may be applied to other similar machines which nevertheless differ somewhat in construction or operation. Changes and modifications of the kit may be required to suit particular requirements. Such variations as are within the skill of the designer, and which do not depart from the true scope and spirit of the invention are intended to be covered by the following claims.

What is claimed is:

1. A code reader kit for use with a letter sorting machine having an input console which includes an operator-controlled keyboard for the entry of destination data for each mail piece and a ZIP mail translator (ZMT) for converting such data into a sort bin designation, comprising in combination:

a code reader operatively mounted on said console for reading pre-coded address information on each said mail piece,

a ZIP data input interface coupled between said code reader and said ZMT, said ZIP data input interface including a data register coupled to said code reader for storing in binary form said address information, binary-to-BCD converter means coupled to said data register for converting said address data to a BCD format, interpreter means, programmable input means coupled to said interpreter means and adpated to be operator programmed with a plurality of predetermined first sequences of digits representative of key assignments on said keyboard, means for coupling a second predetermined sequence of digits from the output of said binary-to-BCD converter means into said interpreter means, said interpreter means comparing said second sequence of digits with said first sequences of digits and providing output signals indicative of the comparisons, transmit control

means including an encoder and memory means for storing predetermined data transmission formats, an operator-selectable digit mode means providing an output signal indicative of the fixed number of digits selected, means for applying the respective outputs of said interpreter and said digit mode means concurrently to said encoder of said transmit control means, means coupling the output of said encoder to said memory means, said last mentioned output providing an address in said memory means and one of said transmission formats, a pair of digit select means, means for coupling all of said address data from said binary-to-BCD converter means to each of said pair of digit select means, means coupling an address and enable signal from said memory means to both said digit select means for selecting a digit to be transmitted to said ZMT, and a pair of BCD-to-decimal converter means coupled respectively to said digit select means for converting said last mentioned digit to decimal form prior to its transmission to said ZMT.

2. A code reader kit as defined in claim 1 further characterized in that said programmable input means of said ZIP data input interface comprises a set of BCD switches, each switch representing a decimal digit, said BCD switches providing output signals indicative of the switch settings.

3. A code reader kit as defined in claim 2 wherein said interpreter means includes a multiplexer, a decade counter and a comparator, said multiplexer being coupled to said set of BCD switches for receiving the output signals therefrom, said multiplexer being further coupled to said decade counter and being sequentially addressed thereby such that multiplexer signals are generated corresponding to said plurality of predetermined first sequences of digits, said comparator means being coupled to both said multiplexer and said binary-to-BCD converter means whereby said plurality of first sequences of digits are compared to said second sequence of digits derived from said last mentioned converter means, means connecting said comparator to said decade counter for terminating the sequential addressing of said multiplexer in response to the occurrence of a match in first and second sequence digits, the address into said multiplexer at the time of said match being representative of the decimal number of the key on said keyboard assigned to the code producing the match, said multiplexer generating a special output digit indicative of the last mentioned address.

4. A code reader kit as defined in claim 3 further including a timing generator comprised of an oscillator of preselected frequency, a division counter arranged to divide said frequency and a sequence signal shift register, the output of said oscillator being coupled to said decade counter of said interpreter and providing therefor a first clock, said oscillator being further coupled to said division counter which in turn is coupled to said shift register, said shift register providing a sequential plurality of outputs at a second clock generated by said division counter.

5. A code reader kit as defined in claim 4 further characterized in that said means coupling the output of said encoder to said memory means in said transmit control means includes a control counter, the output of said encoder being applied to said control counter for enabling a predetermined BCD code to be loaded thereinto, said BCD code specifying the starting address of the count, the output of said control counter being coupled to said memory means and providing an address therefor which serves as the starting point for the destination format required.

6. A code reader kit as defined in claim 5 wherein said pair of digit select means are a respective pair of multiplexers.

7. A code reader kit as defined in claim 6 wherein said data register is capable of storing 20 bits and said binary-to-BCD converter means comprise a pair of binary-to-BCD converters, a first converter of which provides as an output the first three digits of the ZIP code read by said code reader, said first three digits corresponding to said second sequece of digits applied to said comparator in said interpreter, and a second converter of which, provides as an output, the last two digits of said ZIP code.

8. A code reader kit as defined in claim 7 wherein two of the bits stored in said data register are utilized respectively for a parity and a framing check.

9. A code reader kit as defined in claim 8 further including switching means for selectively placing said console in a manual keyboard mode or an automatic code reader mode.

10. A code reader kit as defined in claim 9 wherein said keyboard of said input console is comprised of a regular section and an auxiliary section, the pair of digit select multiplexers being associated respectively with the last mentioned sections.

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